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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/002,034 | 11/01/2001 | Alexander Saldanha | 21891.02101 | 4992 |

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| EXAMINER | |
|---|---|
| LEVIN, NAUM B | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/002,034 | SALDANHA ET AL. | |
| | Examiner | Art Unit | |
| | Naum B Levin | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *01 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☒ Claim(s) *1,8,13 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claims 1, 8, 13 and 17 are objected to:

the recitation of "cores" and "shells" are not clear to what applicants intend to mean. Additional information should be provided.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3 and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ginetti (US Patent 6,622,291).

Ginetti discloses method and apparatus for physical budgeting during RTL floorplanning including:

(1), (17) A method, computer readable media having stored instructions for synthesizing an integrated circuit design, the method comprising (col.32, ll.20-49):

performing physical optimization of block/cell and wire placement, before performing logic synthesis (col.3, ll.18-35);

partitioning the blocks into cores/logical cells/logic cones and shells/nutshells/physical block (col.3, ll.12-17; col.6, ll.46-67; col.7, ll.1-67; col.8, ll.1-67; col.9, ll.1-1; col.32, ll.56-67; col.32, ll.1-67; col.33, ll.1-10);

synthesizing the shells and cores (col.9, ll.2-18); and

recombining the cores and shells into blocks (loop for physical optimization) (col.3, ll.18-35; col.9, ll.2-18);

(2), (18) The method, wherein performing physical optimization of block placement comprises estimating an area of each block (col.6, ll.46-67; col.7, ll.1-67; col.8, ll.1-67; col.9, ll.1-1; col.14, ll.35-51; col.29, ll.10-19; col.33, ll.58-67);

(3), (19) The method of Claim 2, wherein performing physical optimization of wire placement comprises determining a pin (I/O) assignment layout (col.34, ll.1-26).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-16 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ginetti in view of Groeneveld et al. (US Patent 6,230,304).

5. With respect to claims 4-16 and 20-23 Ginetti teaches method and apparatus for physical budgeting during RTL floorplanning including:

(8) A method for designing integrated circuits, the method comprising:

performing layout of physical blocks by estimating an area for each block (col.6, ll.46-67; col.7, ll.1-67; col.8, ll.1-67; col.9, ll.1-1; col.14, ll.35-51; col.29, ll.10-19; col.33, ll.58-67);

partitioning the blocks into cores and shells (col.3, ll.12-17; col.6, ll.46-67; col.7, ll.1-67; col.8, ll.1-67; col.9, ll.1-1; col.32, ll.56-67; col.32, ll.1-67; col.33, ll.1-10);

synthesizing the shells (col.9, ll.2-18);

synthesizing the cores (col.9, ll.2-18); and

recombining the shells and cores (col.3, ll.18-35; col.9, ll.2-18);

(13) A method for reducing design cycle time for integrated circuits, the method comprising:

laying out blocks by estimating an area for each block (col.6, ll.46-67; col.7, ll.1-67; col.8, ll.1-67; col.9, ll.1-1; col.14, ll.35-51; col.29, ll.10-19; col.33, ll.58-67);

partitioning each block into a core and a shell (col.3, ll.12-17; col.6, ll.46-67; col.7, ll.1-67; col.8, ll.1-67; col.9, ll.1-1; col.32, ll.56-67; col.32, ll.1-67; col.33, ll.1-10);

performing logic synthesis an each shell by utilizing a known delay for each wire (col.9, ll.2-18);

performing logic synthesis on each core (col.9, ll.2-18); and

recombining the shells and cores (col.3, ll.18-35; col.9, ll.2-18).

6. With respect to claims 4-16 and 20-23 Ginetti teaches the features above but lacks a method for designing deep sub-micron integrated circuits further comprising connecting pins of the blocks with no timing constraints and assigning each wire to a metal layer pair.

Groeneveld recites method of designing a constraint driven integrated circuit Layout including:

A method for designing deep sub-micron integrated circuits, the method comprising:

connecting pins of the blocks with no timing constraints (col.6, ll.65-67; col.1, ll.1-67; col.7, ll.1-26);

assigning each wire to a metal layer pair (col.1, ll.35-49; col.5, ll.64-67; col.6, ll.1-10; col.1, ll.1-67; col.9, ll.65-67; col.10, ll.1-22 and ll.52-67; col.11, ll.1-3; col.12, ll.28-43; col.19, ll.65-67; col.20, ll.1-28);

optimizing the speed/delay/timing of each wire for its respective layer (col.9, ll.65-67; col.10, ll.1-22);

minimizing a delay in each global wire (col.9, ll.65- 67; col.10, ll.1-22);

(4), (9), (14), (20) The method, wherein performing physical optimization of wire placement further comprises selecting a layer for each wire based on wire length (col.1, ll.35-50; col.5, ll.64-67; col.6, ll.1-10; col.9, ll.66-67; col.10, ll.1-22 and ll.52-67; col.11, ll.1-3; col.19, ll.65-67; col.20, ll.1-28);

(5)-(7); (10)-(12); (14)-(16); (21)-(23) The method, wherein performing physical optimization of wire placement further comprises minimizing a delay in each wire by inserting buffers at optimal distances (col.9, ll.65-67; col.10, ll.1-22).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Groeneveld's teaching regarding the method for designing deep sub-micron integrated circuits further comprising connecting pins of the

blocks with no timing constraints and assigning each wire to a metal layer pair and use it in Ginetti's invention to improve an efficiency of the deep sub-micron integrated circuit design.

***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bodine et al. (US Patent 6,684,373) discloses method, system, and program product for designing an electronic circuit. The electronic circuit has a source component, a sink component and a wire connecting the source and sink components. In one aspect, the wire is divided into wire segments and repeater buffers are added to connect the wire segments. The number of repeater buffers is based on the calculated delay of the global net. In another aspect, the metal routes of the wire are widened to reduce delays on a global net. In these ways, the timing goal of the electronic circuit is met, such that an operation in the electronic circuit will complete within one clock cycle.

Kim et al. (US Publication No. 20020178432) recites method, system and computer-executable code are disclosed for synthesizing a representation of a circuit into a new circuit representation having greater unateness. The invention includes partitioning a circuit representation to obtain a representation of at least one sub-circuit, recursively decomposing the representation of the at least one sub-circuit into a sum-of-products or product-of-sums representation having greater unateness than the representation of the at least one sub-circuit, merging the sum-of-products or product-of-sums representation into the circuit representation to form a new circuit

representation, and repeating until a desired level of unateness for the new circuit representation is achieved.

Graef et al. (US Patent 6,189,131) describes a method for assigning signals to specific metal layers through the use of interconnect wire load models that are metal layer dependent. The method allows synthesis and layout tools to route signal wires on select metal layers at an early stage in the design process. In addition to traditional library components such as logic gate information, the technology library includes routing wire load models that are metal layer dependent. The wire load information reflects the electrical properties of signal wires formed on different metal layers, and provides more accurate timing estimates than generic wire delay values. The additional information influences the delay calculations of the synthesis process in such a way that the delay a signal encounters on a specific metal layer can be approximated very closely.

Pileggi et al. (US Patent 6,286,128) teaches method for design optimization using logical and physical information is provided. In one embodiment, a method for design optimization using logical and physical information, includes receiving a behavioral description of an integrated circuit or a portion of an integrated circuit, optimizing placement of circuit elements in accordance with a first cost function, and optimizing logic of the circuit elements in accordance with a second cost function, in which the optimizing placement of the circuit elements and the optimizing logic of the circuit elements are performed concurrently. The method can further include optimizing routing in accordance with a third cost function, in which the optimizing routing, the

optimizing placement of the circuit elements, and the optimizing logic of the circuit elements are performed concurrently.

Dupenloup et al. (US Patent 6,421,818) recites method of efficiently characterizing modules of an integrated circuit (IC) design using a logic synthesis tool comprising the steps of defining a list of instances of the modules to characterize, and characterizing entire modules of said list of instances of the modules using a single invocation of characterize command of the logic synthesis tool.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

N L

Ihnando
Patent examiner
AU-2825
4/09/2004